REMARKS

Claims 1-30 remain pending in the present application, and stand rejected under Devine (US 6397242) in view of Dornan (US 7,089,539) and a new reference Waldspurger (US 7,260,820). Applicants acknowledge the withdrawal of the prior rejections based on Devine (US 6,397,242) in view of Dornan (US 7,089,539), and the withdrawal of the prior 35 USC Section 112 rejections. Reconsideration of this application is respectfully requested in view of the above claim amendments and the arguments presented below.

Claim Objections

Applicants have amended Claims 5, 15, and 25 in response to the cited claim language informalities, thereby overcoming the cited claim objections.

35 U.S.C. Section 103 Rejections

Paragraph 4 of the above referenced Office Action indicates that independent Claims 1, 11, and 21 are rejected under 35 USC Section 103 as being rendered obvious by Devine (US 6397242) in view of Dornan (US 7,089,539) and a new reference Waldspurger (US 7,260,820). Applicants respectfully traverse the rejection by pointing out that the rejection fails to establish a prima facie case of obviousness since the combined references fail to teach each and every element of the claims.

Each of the independent claims recite aspects regarding the micro architecture code with respect to the processor architecture. With respect to Claim 1, Claim 1 recites a method for supporting input/output for a virtual machine, comprising:

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executing virtual machine application instructions of a virtual machine application by using micro architecture code of a processor architecture;

receiving an I/O access from the virtual machine application at a monitor supporting the virtual machine application;

in response to receiving the I/O access, generating an exception;

performing the I/O access by using a host operating system configured to support the monitor;

updating state data for the virtual machine application at the monitor in accordance with the I/O access, the updating performed by a virtual machine component of the micro architecture code; and

resuming execution of the virtual machine application from the exception. (emphasis added)

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As explicitly recited in Claim 1, virtual machine application instructions of a virtual machine application are executed by using micro architecture code of a processor architecture (emphasis added). The state data for the virtual machine application is subsequently updated at the monitor in accordance with the I/O access, and the updating is performed by a virtual machine component of the micro architecture code (emphasis added). Applicants point out that those skilled in the art are aware that micro architecture code of a processor is not available to programs executing on top of the processor (e.g., x86 architecture, etc.). This micro architecture code is directly processed by the pipelines of the CPU. Accordingly, this micro architecture code is not

available outside the processor environment and it cannot be accessed outside of the processor environment. Applicants point out that this is very different from, for example, Java byte code (emphasis added). Similar limitations are included in each of the independent Claims 11 and 21.

Paragraph 6 of the above referenced Office Action acknowledges that Devine is silent regarding (e.g., does not show or suggest) the use of micro architecture code of a processor architecture. Dornan is relied upon as allegedly disclosing "a computer system with micro architecture code of a processor code to feed pipelines of the processor architecture hardware, including a hardware instruction interpreter to execute the VM application instructions" (e.g., Dornan Abstract and Dornan col. 1 lines 47-67, and Fig. 11, item 126). However, Applicants point out that Dornan does not show or suggest the state data for the virtual machine application being updated at the monitor in accordance with the I/O access, and the updating is performed by a virtual machine component of the micro architecture code (emphasis added). Applicants assert that Dornan does not show or suggest a virtual machine component of the micro architecture code that updates state data at the monitor for the virtual machine application (emphasis added). Applicants assert that this is because Dornan is directed towards the execution of a Java virtual machine, and therefore the execution of Java byte

code (e.g., Dornan Abstract and Dornan col. 1 lines 47-67, and Fig. 11, item 126). This is completely different from micro architecture code.

The above discussed defect of Dornan and Devine is not cured by the addition of Waldspurger. The above referenced Office Action relies upon Waldspurger to show "I/O operations between virtual machine any device external to the virtual machine are monitored by a virtual machine monitor that receives the I/O access, generates exceptions, and updates state data" (e.g., Waldspurger Fig. 1, items 300, 400, 430, 470, abstract, col. 2 lines 45-57, col. 5 lines 36-67, col. 6 lines 1-10). However, Applicants point out that as with Devine and Dornan, Waldspurger does not show or suggest the state data for the virtual machine application being updated at the monitor in accordance with the I/O access, and the updating is performed by a virtual machine component of the micro architecture code (emphasis added). Applicants assert that the cited combination of Devine, Dornan and Waldspurger do not show or suggest a virtual machine component of the micro architecture code that updates state data at the monitor for the virtual machine application (emphasis added).

Because of the above described rationale, Applicants assert that the cited combination of Devine, Dornan and Waldspurger do not show or suggest a virtual machine component of the micro architecture code that updates

state data at the monitor for the virtual machine application, as recited in Claims 1, 11 and 21. Consequently, Applicants assert that Devine, Dornan and Waldspurger fail to establish a prima facie case of obviousness since the combined references fail to teach each and every element of the claims. Thus, Claims 1, 11 and 21 are not rendered obvious by Devine in combination with Dornan and Waldspurger within the meaning of 35 USC Section 103. Dependent Claims 2-10, 12-20 and 22-30 overcome the cited rejections by virtue of their dependency.

CONCLUSION

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
MURABITO, HAO & BARNES

Dated: August 27, 2009

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